that Claims 1-15, as amended, are patentable for at least the following reasons.

Patterson discloses an analog to digital encoding system with offset and gain correction functions. As shown in FIG 3 of Patterson, the encoding system has an input transconductance amplifier 102 which is connected to a comparator 106. The comparator 106 receives the output of the amplifier 102 and provides an output to a latch 105. A signal sample and hold circuit 116, which doubles as an offset correction sample and hold receives the output of the comparator 106. The output of the sample and hold circuit 116 is fed back to the comparator 106. The Patterson encoding system also has input switches 100 that provide an analog signal or ground to the transconductance amplifier 102 so that the sample and hold circuit 116 can measure either the signal level or ground.

In stark contrast, the inventive signal processing system as recited in independent Claims 1 and 12 has means to temporarily fix the level of <u>two</u> signals, e.g., at zero or ground as shown in FIG 4 and described on page 7 lines 17-23 of the specification. The two signals are the analog input signal at the system input, and the analog correction signal at the second input of the combining means.

In addition, the inventive signal processing system and method, as recited in independent Claims 8 and 9

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includes a subtracting circuit, shown in FIG 4 as reference numeral 306 for example. The subtracting circuit 306 has two inputs, namely, the analog input signal and the analog correction signal and a difference output, which is the difference between its two inputs.

Further, as specifically recited in Claims 8 and 9, the inventive signal processing system includes an array of switches connected between a ladder of resistors and an output node of the switch array, which output node is connected to the second input of the combining circuit. A control logic is provided for controlling the switches.

A subtracting circuit along with the particular cooperation among the array of switches, the ladder of resistors, the control logic and the subtracting circuit recited in Claims 8 and 9, and the means to temporarily fix the level of two signals, as recited in Claims 1 and 12, are not disclosed or suggested in Patterson.

Mangelsdorf and Suarez do not remedy these deficiencies in Patterson. In particular, Mangelsdorf is cited to show a multi-stage A/D converter, while Suarez is cited to show control means for controlling a digital-to-analog switching circuit. There is no teaching or suggestion in Patterson, Mangelsdorf, Suarez or combination thereof, of the temporarily fixing means or the particular arrangement of the switch array, resistor ladder, control

means and subtracting circuit recited in independent Claims 1, 8, 9 and 12 of the present invention.

Accordingly, it is respectfully requested that the rejections under 35 U.S.C. §103(a) of Claims 1-15 be withdrawn, and independent Claims 1, 8, 9 and 12 be allowed over the prior art of record. In addition, since Claims 2-7, 11 and 13-15 depend from the independent Claims 1, 8, 9 and 12, Applicant respectfully requests that Claims 2-7, 11 and 13-15 also be allowed over the prior art of record.

It is respectfully submitted that Claims 6 and 11 also contain patentable subject matter. In particular, Claims 6 and 11 recite a further array of multiple further switches, as shown in FIG 10. Two arrays of switches in the manner recited in Claims 6 and 11 are nowhere taught or suggested in any of the references of record, or combination thereof.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

If any informalities remain, the Examiner is requested to telephone the undersigned in order to expedite allowance.

Please charge any fee deficiencies and credit any overpayments to Deposit Account No. 14-1270.

Respectfully submitted,

By _____
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(914) 333-9607
June 1, 1998

Enclosure: Proposed Drawing Corrections (FIGs 1-3, 6 and 11-13, 6 sheets)

CERTIFICATE OF MAILING

It is hereby certified that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to:

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On June 1, 1998

By _____